

STACKUP TABLE:

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.80mil	3.5	
1	L1 TOP	Copper	1.60mil		
	Dielectric 1	R03003 core, 17um, rolled copper	5.00mil	3	
2	L2 GND	Copper	0.80mil		
	Dielectric2	R04450F	5.00mil	4.2	
3	L3 SIGNAL 1	Copper	0.60mil		
	Dielectric3	R04835 core 17um, LoPro copper	10.70mil	3.66	
4	L4 GND	Copper	0.60mil		
	Dielectric4	370HR	5.00mil	4.2	
5	L5 SIGNAL 2	Copper	1.20mil		
	Dielectric5	370HR	10.00mil	4.34	
6	L6 SIGNAL 3	Copper	0.60mil		
	Dielectric6	370HR	5.00mil	4.2	
7	L7 GND	Copper	0.80mil		
	Dielectric7	370HR	5.00mil	4.34	
8	L8 BOTTOM	Copper	1.60mil		
	Bottom Solder	Solder Resist	0.80mil	3.5	
	Bottom Overlay				

THIS IS AN IMPEDANCE CONTROLLED BOARD

NOTE:

1. EXTERNAL LAYER CU THICKNESS ARE FINISHED THICKNESS AFTER PLATING.

NOTES: UNLESS OTHERWISE SPECIFIED.

1. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
2. THE SOLDER MASK IMAGES THAT ARE THE SAME SIZE AS THE COMPONENT PADS MAY BE ENLARGED AS PER THE MANUFACTURING CAPABILITIES BUT NOT BEYOND 0.08MM PER SIDE OR 0.15MM OVERALL.
- ALL OTHER SOLDER MASK IMAGES SHALL NOT BE MODIFIED.
3. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL FOR ETCHING ACCURACY NEAR THE ANTENNA REFER "ANTENNA_ETCHING_REQUIREMENTS" DOCUMENT
4. 5.9MIL VIA ONLY ON PAD SHOULD BE FILLED WITH CONDUCTIVE COPPER AND SURFACE SHOULD BE FLAT. FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON TOP SIDE.
5. BACKDRILLING INFO: 12 MIL DRILL AND 24 MIL PAD NEED TO BE REMOVED FROM THE BOTTOM TO LAYER 4 USE 24MIL DRILL BIT FOR BACKDRILLING ABOVE MENTIONED DRILLS. VENDOR MUST CUT L4 AND MUST NOT CUT L3.
6. PRINTED WIRING BOARD SHALL COMPLY WITH REQUIREMENTS OF ANSI/J-STD-003.
7. BOW AND TWIST SHALL NOT EXCEED 0.7% OF LONGEST SIDE
8. R136/R140 REQUIRE SPECIAL ASSEMBLY ATTENTION DUE TO THEIR NO SOLDER-MASK, RF CONSTRUCTION.
9. FOR ANY ASSEMBLY OR FABRICATION QUESTIONS PLEASE CONTACT THE RESPONSIBLE TI PCB DESIGN TEAM.

IMPEDANCE TABLE

LAYER	TRACE WIDTH (mil)	TRACE SPACING (mil)	IMPEDANCE
1	10.5	-	50 OHM +/-10%
1	6.5	5.5	100 OHM +/-10%
3	5.1	-	50 OHM +/-10%
5	12	-	50 OHM +/-10%
6	6.9	-	50 OHM +/-10%
6	5	7	100 OHM +/-10%
8	7.75	-	50 OHM +/-10%
8	5.25	6.75	100 OHM +/-10%

Symbol	Count	Hole Size	Drill Layer Pair	Plated	Hole Tolerance(mil)
L	60	7.87mil (0.200mm)	L1 TOP - L8 BOTTOM	PTH	+0/-7.87
B	727	8.00mil (0.203mm)	L1 TOP - L8 BOTTOM	PTH	+0/-8
C	13	12.00mil (0.305mm)	L1 TOP - L8 BOTTOM	PTH	+0/-12
D	1522	12.20mil (0.310mm)	L1 TOP - L8 BOTTOM	PTH	+0/-12.2
E	8	39.37mil (1.000mm)	L1 TOP - L8 BOTTOM	PTH	+4/-0
F	8	40.00mil (1.016mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
G	8	47.24mil (1.200mm)	L1 TOP - L8 BOTTOM	PTH	+4/-0
H	6	70.87mil (1.800mm)	L1 TOP - L8 BOTTOM	PTH	+/-2
I	2	118.11mil (3.000mm)	L1 TOP - L8 BOTTOM	NPTH	+/-2
J	4	118.11mil (3.000mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
K	4	160.00mil (4.064mm)	L1 TOP - L8 BOTTOM	PTH	+/-3
	2362 Total				

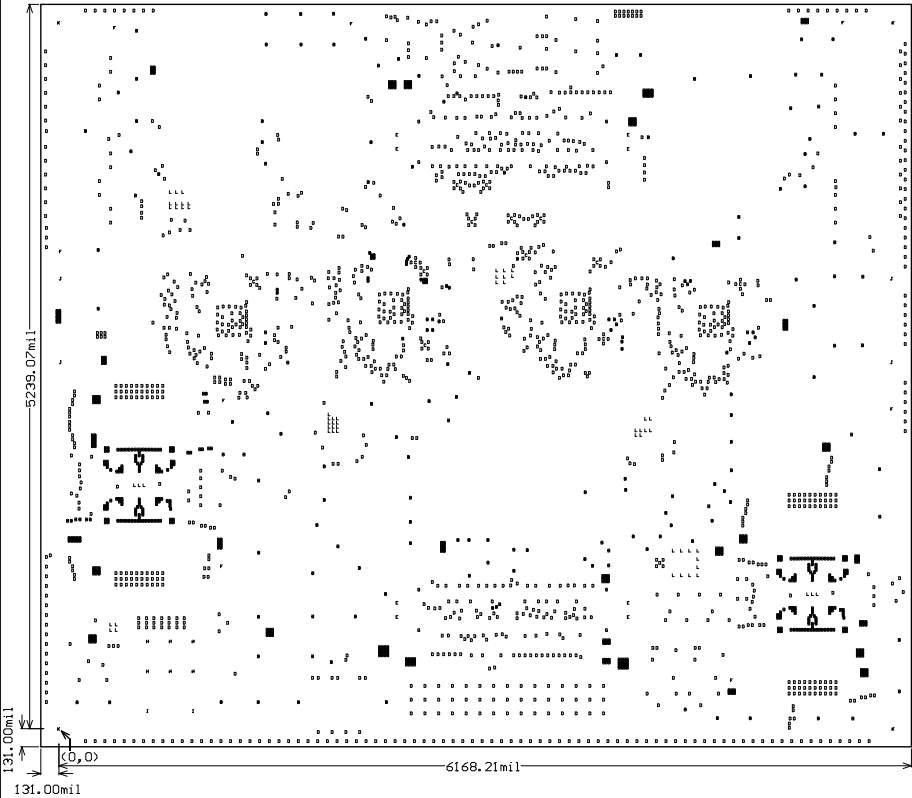
DRILL TABLE: (L1-L8)

DESIGN INFORMATION	
MIN. TRACK WIDTH: 4 MIL	
MIN. CLEARANCE: 4 MIL	
MIN. VIA PAD SIZE: 13.72 MIL	
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 2 MIL, HOLES +/- 3 MIL	
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input type="checkbox"/> FR-4 High Tg <input checked="" type="checkbox"/> OTHER REFER STACKUP	
THICKNESS: <input type="checkbox"/> 62 MIL (1.6mm) +/-10% <input checked="" type="checkbox"/> OTHER 55MIL +/-10%	
TOLERANCE: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	
<input type="checkbox"/> OTHER +/-	
BOW & TWIST: <input type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	
<input checked="" type="checkbox"/> OTHER +/- REFER NOTE 7	
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES	
PTH COPPER THICKNESS: <input checked="" type="checkbox"/> 20-30 um <input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER	
SOLDER RESIST COLOR: <input type="checkbox"/> GREEN <input checked="" type="checkbox"/> OTHER RED	
<input type="checkbox"/> MATTIE <input type="checkbox"/> SEMI-GLOSS	
SURFACE FINISH: <input type="checkbox"/> IMMERSION GOLD (ENG) <input type="checkbox"/> ENEPG	
<input checked="" type="checkbox"/> IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL: <input type="checkbox"/> CUT AND TRIM PER M1 BOARD OUTLINE	
<input type="checkbox"/> N.C. ROUTE <input type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs	
TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3	
<input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.	
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER	
ADDITIONAL REQUIREMENTS:	
MICROSECTION: <input type="checkbox"/> YES	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
<input type="checkbox"/> XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE	
<input type="checkbox"/> OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE	
<input type="checkbox"/> LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE	
TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE	



PROJECT TITLE:	
MMWCAS-RF-EUM	
DESIGNED FOR:	
Public Release	
FILE NAME:	
PROC054D_MMWCAS_RF_EUM_PcbDoc	
ENGINEER:	LAYOUT BY:
a0271760	Tessolve/TI
SCALE: 0.54	ALTM DESIGNER VERSION:
	19.1.9.167

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ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC054	REV: D	SUN REV: 550b393939fce2f9ed30b80f1740aebef4e0ee049 [Locally Modified]
LAYER NAME = R03003 core, 17um, rolled copper			
GENERATED : 6/18/2020 6:41:12 PM	TEXAS INSTRUMENTS		

